SINGLE INSTRUCTION FOR MULTIPLE LOOPS

Abstract

Embodiments of the present invention relate generally to the manner in which processors execute multiple loop instructions. That is, embodiments of the invention relate to the organization of multiple loop constructs, such as, for example, nested loops, to achieve improved performance during loop execution. One embodiment contemplates a single instruction that provides for execution of other instructions of a set of instructions in accordance with multiple looping constructs. Another embodiment contemplates a single-loop instruction suitable for terminating on multiple termination conditions.